

Inventor: Yasuaki HIRANO

Title: ERASE METHOD FOR NONVOLATILE  
SEMICONDUCTOR STORAGE DEVICE AND ROW  
DECODER CIRCUIT FOR FULFILLING THE METHOD

## REPLACEMENT SHEET

Fig. 11A

a0~a13 BA

BA: BLOCK ADDRESS

erssetup Vcc

Vss

Fig. 11B

erssetupb Vcc

Vss

Fig. 11C

hnrset Vcc

Vss

Fig. 11D

hnrneg1, hnrneg Vcc

Vss

Fig. 11E

hhvpre Vcc

Vpp

Fig. 11F

hhvpre1 Vcc

Vss

Fig. 11G

hnrpx Vss

Vpp

Fig. 11H

hnrns Vss

Vneg

Fig. 11I

xnrwb Vss

Vss

Fig. 11J

xnrwb Vcc

Vss

Fig. 11K

WL0~WL31 Vss

Vpp

Fig. 11L

WL32~ WL16383 Vss

Vneg

Fig. 11M

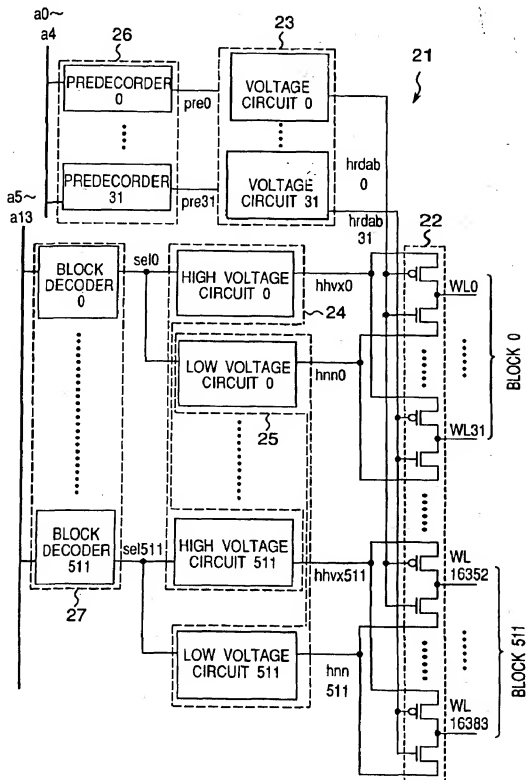
Approved  
10/17/03

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SEP 08 2003  
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Docket N. : 204552018400

# Fig.12 REPLACEMENT SHEET



## REPLACEMENT SHEET

Fig.13

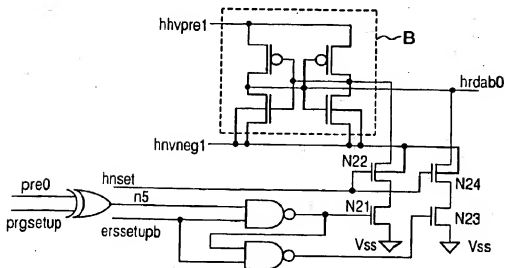
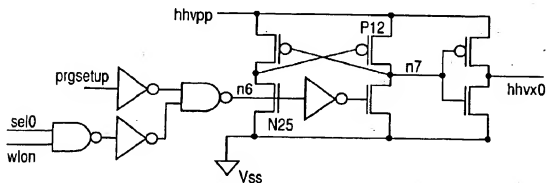


Fig.14

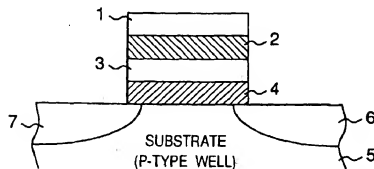




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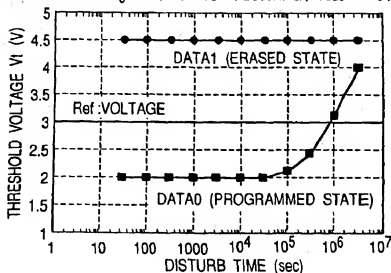
## REPLACEMENT SHEET

*Fig.19 PRIOR ART*



*Fig.20 PRIOR ART*

CONDITIONS :  $V_g=0V$ ,  $V_d=V_s=$  FLOATING,  $V_{sub}=-8V$





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# REPLACEMENT SHEET

Fig.21 PRIOR ART

